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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/646,530

08/23/2003

John Groe

SECO-018/01US

8492

23419

7590

11/21/2006

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EXAMINER

PHU, PHUONG M

ART UNIT

PAPER NUMBER

2611

DATE MAILED: 11/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/646,530

Applicant(s)

GROE ET AL.

Examiner

Phuong Phu

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 23 August 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-12 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-12 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____.
- ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- ☐ Notice of Informal Patent Application
- ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

1. The oath or declaration is defective. A new oath or declaration in compliance with 37 CFR 1.67(a) identifying this application by application number and filing date is required. See MPEP §§ 602.01 and 602.02.

The oath or declaration is defective because:
It does not identify the citizenship of inventor Joseph Austin.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Gersbach et al (5,508,660).

-Regarding to claim 1, see figures 1 and 2, and col. 3, line 30 to col. 6, line 9, Gersbach et al discloses a charge pump circuit (see figure 2), comprising:

a replica circuit (comprising (T7, T8)) that provides at node (49) a current difference between charge up and discharge down currents (outputted from (T7, T8)) to node (49) (see col. 5, lines 24-40); and

a buffer (46) coupled to the replica circuit to buffer a received control voltage (V_{RC}) (see col. 5, lines 5-22).

-Regarding to claim 2, see figures 1 and 2, and col. 3, line 30 to col. 6, line 9, Gersbach et al discloses a charge pump circuit for use in a phase-lock loop circuit, the charge pump circuit (see figure 2) comprising:

a charge pump core circuit (comprising (H4, H12)) that outputs via (H17, H3)) a control voltage (V_{RC}) (see col. 4, line 40 to col. 5, line 5);

a replica circuit (comprising (T7, T8)) that is coupled to the charge pump core circuit, wherein the replica circuit receives (via (T4, T5)) the control voltage and produces (via (42, 44)) one or more bias signals ("error current" (outputted from (T2, T1)) (see col. 5, lines 50-51) that are coupled to the charge pump core circuit to minimize the difference between charge up and charge down currents generated (from H4, H12) by the charge pump core circuit (see col. 5, line 6 to col. 6, line 9).

-Regarding to claim 3, Gersbach et al discloses a buffer circuit (46) that is coupled to receive the control voltage and output the control voltage to the replica circuit (see figure 2).

-Regarding to claim 4, Gersbach et al discloses one or more error circuits (42, 44), (considered here equivalent with the limitation "error amplifiers"), that are coupled to the replica circuit and the buffer circuit, the one or more error amplifiers operate to output the one or more bias signals (see col. 5, lines 40-55).

-Regarding to claim 5, Gersbach et al discloses (see figure 2):

a combination circuit (inherently included at the intersection node of (H4, H17, T2) for combining a charge up current outputted from (H4) and a bias current outputted from (T2), (the combination circuit considered here equivalent to the limitation "servo circuit"), coupled to the replica circuit to receive at least one bias signal (outputted from (T2)); and

a driver circuit (H17) coupled between the servo circuit and the charge pump core circuit.

-Regarding to claim 6, as similarly applied to claims 1-5, set forth above and herein incorporated, see figures 1 and 2, and col. 3, line 30 to col. 6, line 9, Gersbach et al discloses a method (see figure 2) for operating a charge pump circuit in a phase-lock loop circuit, the method comprising:

procedure (H4, H17, H3, H12) of generating an output control voltage (V_{RC}) at a charge pump core circuit (30);

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procedure (42, 44) of generating one or more bias signals (outputted from (T1, T2) based on the control voltage; and

procedure (H4, H17, H3, H12) of adjusting the operation of the core circuit based on the one or more bias signals so as to minimize a difference between charge up and charge down currents (generated from (H4, H12)).

-Regarding to claim 7, Gersbach et al discloses that generating the one or more bias signals comprises (see figure 2):

procedure (46) of receiving the control voltage at a buffer circuit (46) that outputs a version (47) of the control voltage; and

procedure (T4, T5) of receiving the version of the control voltage at a replica circuit (T4, T5, T7, T8, 42, 44) that generates the one or more bias signals based on the control voltage.

-Regarding to claim 8, Gersbach et al discloses (see figure 2):

procedure (46, T4, T5) of generating a current difference (outputted from (T4, T5) based on the version of the control voltage; and

procedure (42, 44) of generating the one or more bias signals based on the current difference.

-Regarding to claim 9, as similarly applied to claims 1-4, set forth above and herein incorporated, see figures 1 and 2, and col. 3, line 30 to col. 6, line 9, Gersbach et al discloses a charge pump circuit (see figure 2) for use in a phase-lock loop circuit, the charge pump circuit comprising;

a charge pump core circuit means (comprising (H4, H12))) for outputting (via (H17, H3)) a control voltage (V_{RC});

a replica circuit means (T4, T5, T7, T8, 42, 44) for receiving the control voltage and producing one or more bias signals (outputted from (T1, T2) that are coupled to the charge pump core circuit

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means to minimize the difference between charge up and charge down currents generated from (H4, H12)) by the charge pump core circuit means.

-Regarding to claim 10, Gersbach et al discloses a buffer circuit means (46) for receiving the control voltage and outputting a version (47) of the control voltage to the replica circuit means (see figure 2).

-Regarding to claim 11, Gersbach et al discloses one or more error amplifiers means ((42, T4), (44, T5)) for receiving the version of the control voltage and outputting the one or more bias signals (see figure 2).

-Regarding to claim 12, Gersbach et al discloses (see figure 2):

a combination circuit (inherently included at the intersection node of (H4, H17, T2), (the combination circuit considered here equivalent with the limitation "servo circuit means"), for receiving the at least one bias signal; and

a driver circuit means (H17) coupled to the servo circuit means.

Conclusion

4. References 5945855 and 6781425 are additionally cited because they are pertinent to the claimed method and associated system.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phuong Phu whose telephone number is 571-272-3009. The examiner can normally be reached on M-F (8:00 AM - 4:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on 571-272-2988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Phuong Phu
10/27/06**PHUONG PHU
PRIMARY EXAMINER**Phuong Phu
Primary Examiner
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